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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,452	07/16/2003	Yoshiyuki Teshirogi	Q76534	7704

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
BODDIE, WILLIAM	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/619,452	TESHIROGI ET AL.	
	Examiner	Art Unit	
	William L. Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-6,8 and 9* is/are allowed.

6)☒ Claim(s) *1,2,7 and 10-17* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper.No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, February 5th, 2007, the Applicant amended claims 4, and 11 and added new claims 16-17. Claims 1-17 are currently pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 5th, 2007 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-2 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

4. The drawings were received on February 5th, 2007. These drawings are acceptable.

Claim Objections

5. Claim 15 is objected to because of the following informalities: claim 15 currently states, "wherein aid determining steps." The Applicants appear to have intended this phrase to read, 'wherein said determining step', as the word "aid" is not appropriate in the context, as well as noting that there is only a single determining step in independent claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 11-14 and 16-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Specifically, independent claim 11, requires in part for the delay of a single odd and even numbered bit and subsequently the comparison of said delayed odd and even bits with other odd / even bits. The Examiner was unable to locate any enabling discussion within the specification detailing the delaying of odd bits and subsequently using the delayed bits in a comparison operation.

As claims 12-14 depend from claim 11, and inherit all the limitations from claim 11, they are seen as failing to comply with the enablement requirement for the same reasons shown above.

Claim 16, seems to alter one of the previous comparing steps from independent claim 10. However, the Examiner was unable to locate any enabling discussion or drawings which detail comparison of odd and even numbered bits both being second video data, as described in claim 10.

Claim 17 as currently written requires that a comparator be configured to compare odd and even numbered bits of video data, wherein the video data is identical. The Examiner was once again unable to locate any discussion within the Applicants' disclosure regarding comparing *identical* video data.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

9. Claims 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 currently reads, "wherein said comparing step." It is unclear as to which comparing step the Applicants are referring in this claim, as claim 10, contains two comparing steps.

Claim 17 currently calls for the first comparator to compare even bits of "former video data" with odd bits of "latter video data." It is unclear as to what chronological relationship the two pieces of video data are to one another. It is the current position of the Examiner that "former" and "latter" have identical meanings. As such the limitations of the current claim 17 are indefinite.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 2, 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (US 6,628,256) in view of Honma et al. (US 7,136,110).

With respect to claim 1, Nishimura discloses, a video data transfer method of a display device comprising:

determining whether a bit inversion number between first data (dc1 to 24 in fig. 4) and second data (da1 to 24 in fig. 4) following said first data of output video data is more than half or not; and

inverting a logic state of said second data if the bit inversion number is more than half (col. 8, lines 63-67 col. 9, lines 1-5).

Nishimura does not expressly disclose, converting input video data that is composed of parallel data into partially serialized output video data.

Honma discloses, converting input video data (b7-b0 in fig. 9) that is composed of parallel data into partially serialized (col. 12, lines 16-43; col. 32, lines 16-25) output video data (166-172 in fig. 9).

Honma and Nishimura are analogous art because they are both from the same field of endeavor namely, control circuitry for video data.

At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the partial serialization of Honma in the inversion detection of Nishimura. This would be accomplished by using the P/S (34 in fig. 1) of Honma and adjoining it to the outputs of Nishimura's fig. 2.

The motivation for doing so would have been to decrease the number of wirings to the signal driver and achieve circuit miniaturization (col. 3, lines 24-34; col. 12, lines 28-43).

With respect to claim 2, Nishimura discloses, a video data transfer method comprising:

controlling every $3x2^{(n-m)}$ bits (see 12 in fig. 4, n=4 m=1) a polarity of bits of said input video data that corresponds to said output video data (see dd1to 24 in fig. 4) so that the bit inversion number between first data and second data following said first data of the $3x2^{(n-m)}$-bit parallel of said output video data is $3x2^{(n-m-1)}$ or less (for an example of Nishimura's process see col. 8, lines 62-67 – col. 9, lines 1 –5; states that half of the data ($3x2^{(n-m-1)}$) has to be inverted from previous to subsequent data to trigger the polarity inversion).

Nishimura further discloses, input video data of $3x2^{n}$-bit parallel (24 bit parallel; 3x8).

Nishimura does not expressly disclose, a video data transfer method of display device comprising:

serializing input video data of a $3x2^{n}$-bit parallel in a 2^{m}-bit unit (n and m: natural numbers larger than zero, n>m) to produce output video data of a $3x2^{(n-m)}$-bit parallel.

Honma discloses serializing input video data of a 2^{n}-bit parallel (2^{3}-bit input into fig. 9) in a 2^{m}-bit unit (m=1; col. 12, lines 16-17) (n and m: natural numbers larger than zero, n>m) to produce output video data of a $2^{(n-m)}$-bit parallel ($2^{(3-1)}$-bit output of fig. 9).

While Honma performs dot sequential driving and thus only supplies the 8 bits of each color, R, G and B sequentially, it should be noted that it is Nishimura that the invention of Honma is being incorporated into. As Nishimura does not implement dot sequential driving, it seems obvious to the Examiner that one of ordinary skill would be able to adapt the device of Honma to convert each 8 bits of R, G and B in parallel.

Upon the combination, it should be clear that 3x8 data bits from Nishimura would be supplied to the P/S device of Honma which would in turn output 3x4 data bits of partially serialized data.

As such, at the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the partial serialization means of Honma (fig. 9) on the output buses of Nishimura (note Nishimura, col. 9, lines 48-57).

The motivation for doing so would have been to decrease the number of wirings to the signal driver and achieve circuit miniaturization (col. 3, lines 24-34; col. 12, lines 28-43).

With respect to claims 7 and 15, Honma and Nishimura disclose, the video data transfer method as claimed in claims 1 (see above).

As to the further limitations requiring that the determining step and any subsequent polarity inversion take place prior to the data being partially serialized, the combination of the two pieces of art as described in the above rejection of claim 1 would result in this order of operations.

To further explain, the manipulation of the raw pixel data performed in the resizing circuit (20 in fig. 1) of Honma can be seen as data correction (similar to

Nishimura's polarity inversion). The output data from that data correction circuit is in turn partially serialized. It would have been obvious to one of ordinary skill in the art to in turn perform the partial serialization of data subsequent to the polarity inversion determination of Nishimura.

12. Claims 10-12 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (US 6,628,256) in view of Wright et al. (US 6,550,026).

With respect to claim 10, Nishimura discloses, a video data transfer method of a display device (fig. 4), the method comprising:

comparing (11 in fig. 4) first data and second data (fig. 4) to output an inversion determination signal (inv2 in fig. 4) if first video data is to be inverted (col. 8, line 62 – col. 9, line 4).

Nishimura does not expressly disclose, comparing individual odd bits with even bits, regardless of whether the odd / even bits are first video data or second video data. Nishimura also doesn't disclose comparing bits of first video data with other bits of first video data.

Wright discloses, comparing odd numbered bits of first video data with even number bits of said first video data (col. 8, lines 45-48).

Wright and Nishimura are analogous art because they are both directed to a similar problem solving area, namely efficient bit data comparison.

At the time of the invention it would have been obvious to one of ordinary skill in the art to compare the odd bits with the even bits as taught by Wright in the data transfer method of Nishimura.

The motivation for doing so would have been, to reduce the number of compare circuits required (Wright; col. 3, lines 33-35).

With respect to claim 11, Nishimura discloses, a display control circuit comprising:

a delay circuit (13-1 in fig. 4) which is configured to delay first bits corresponding to one of odd numbered bits and even numbered bits of video data (input into D) and to output the delayed first bits (Q);

a first comparator (11 in fig. 4) which is configured to compare said delayed first bits and second bits (upper input into 11) corresponding to the other of said odd numbered bits and even numbered bits of the video data; and

a second comparator (note the several blocks 10-1-10-4 each of which contain comparators).

Nishimura does not expressly disclose, comparing individual odd bits with even bits. Nishimura also doesn't disclose a second comparator to compare bits of first video data with other bits of first video data.

Wright discloses, comparing odd numbered bits of first video data with even number bits of said first video data, as well as comparing said first bits which are not delayed with second bits (col. 8, lines 6-9, 45-48; col. 7, lines 63-67).

Wright and Nishimura are analogous art because they are both directed to a similar problem solving area, namely efficient bit data comparison.

At the time of the invention it would have been obvious to one of ordinary skill in the art to compare the odd bits with the even bits as taught by Wright in the data transfer method of Nishimura.

The motivation for doing so would have been, to increase the speed of data comparison (Wright; col. 3, lines 9-12).

With respect to claims 12, Nishimura and Wright disclose, the display control circuit as claimed in claim 11 (see above).

Nishimura further discloses, a first control circuit which controls a polarity of said second bits based on the output of said first comparator (12 in fig. 4); and

a second control circuit (10-2 in fig. 2) which controls a polarity of said first bits which are not delayed by said delay circuit based on the output of said second comparator (the inclusion of a second control circuit would have been obvious given the combination of Nishimura and Wright).

With respect to claim 16, Nishimura and Wright disclose, the video data transfer method as claimed in claim 10 (see above).

Nishimura further discloses, outputting the inversion determination signal (inv2 in fig. 4) for determining whether or not the data bits of the second video data are inverted (col. 8, line 62 – col. 9, line 4).

Wright further discloses, comparing the odd numbered bits of the second video data with the even numbered bits of the second bits of the second video data (col. 8, lines 45-48).

Please also note the above rejection of claim 16, under 35 U.S.C. 112.

With respect to claim 17, Nishimura and Wright disclose, the video data transfer method as claimed in claim 11 (see above).

Wright further discloses, wherein said first comparator is configured to compare the even numbered bits of former video data with the odd numbered bits of latter video data different from this (col. 8, lines 45-48); and

wherein said second comparator is configured to compare the even numbered bits of video data wit the odd numbered bits of video data, said video data both being identical (col. 7, lines 63-67; col. 8, lines 6-8).

Please also note the above rejection of claim 17, under 35 U.S.C. 112.

13. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura (US 6,628,256) in view of Wright et al. (US 6,550,026) and further in view of Honma et al. (US 7,136,110).

With respect to claims 13 and 14, Nishimura and Wright disclose, the display control circuit as claimed in claim 12 (see above).

Neither Nishimura nor Wright expressly disclose a data parallel to serial converter which is configured to receive the outputs of said first and second control circuits or first and second comparators and to convert parallel video data including said first and second bits to serial video data.

Honma discloses, converting input video data (b7-b0 in fig. 9) that is composed of parallel data into partially serialized (col. 12, lines 16-43; col. 32, lines 16-25) output video data (166-172 in fig. 9).

Honma, Wright and Nishimura are analogous art because they are all from the same field of endeavor namely, control circuitry for data.

At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the partial serialization of Honma in the inversion detection of Nishimura and Wright. This would be accomplished by using the P/S (34 in fig. 1) of Honma and adjoining it to the outputs of Nishimura's fig. 2.

The motivation for doing so would have been to decrease the number of wirings to the signal driver and achieve circuit miniaturization (col. 3, lines 24-34; col. 12, lines 28-43).

Allowable Subject Matter

14. Claims 3-6 and 8-9 are allowed.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will L. Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

wlb
4/10/07

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER